Sub B1

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ABSTRACT OF THE DISCLOSURE

A method of laying out traces for connection of bond pads of a semiconductor chip to a printed wiring board or the like and the layout. There is provided a substrate having top and bottom surfaces with a plurality of rows and columns of vias extending therethrough from the top surface to the bottom surface and having a solder ball secured at the bottom surface to each via. A plurality of pairs of traces is provided on the top surface, each trace of each pair of traces extending to a different one of the vias and extending to vias on a plurality of the rows and columns, each of the traces of each pair being spaced from the other trace by a ball pitch, being maximized for identity in length and being maximized for parallelism and spacing. Each of the traces of a pair is preferably be further maximized for identity in cross-sectional geometry. A differential signal pair is preferably applied to at least one of a pair of traces. The layout can further include a further surface between the top and bottom surfaces insulated from the top and bottom surfaces, a plurality of the traces being disposed on the further surface.